Title: ANALOG ELECTRONIC CLOCK
Inventor(s): Isao KITAZAWA et al.
DOCKET NO.: 062800-0118

FIG.1

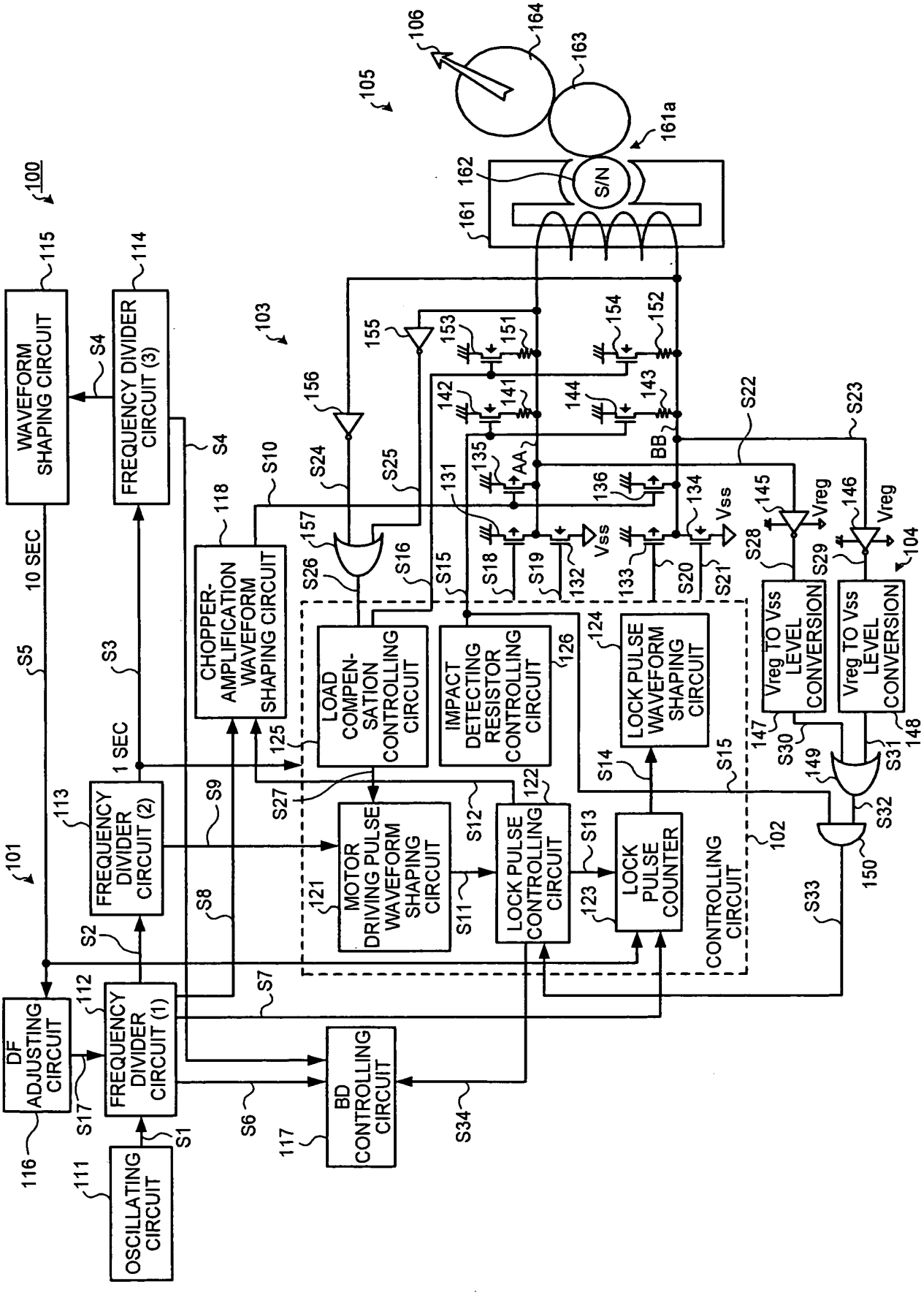

FIG.2

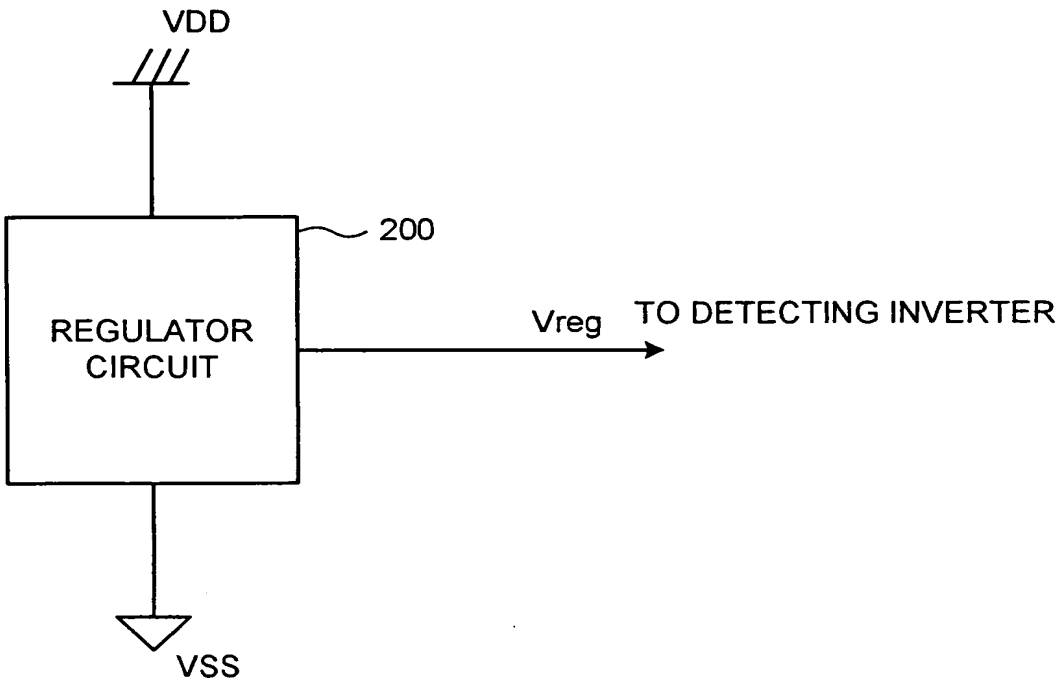

FIG.3

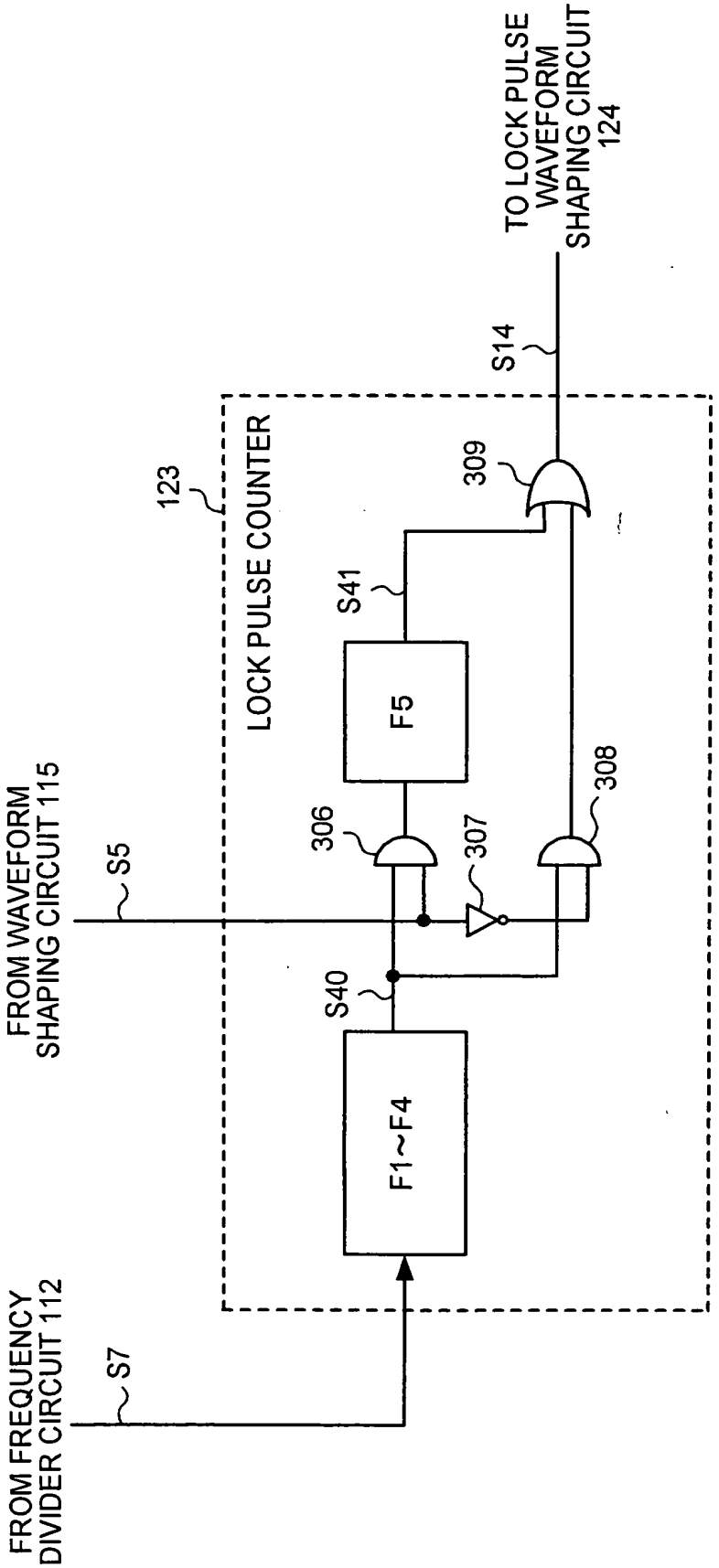
FROM FREQUENCY DIVIDER CIRCUIT 112
S7
FROM WAVEFORM SHAPING CIRCUIT 115
S5
123
LOCK PULSE COUNTER
F1~F4
S40
F5
S41
306
307
308
309
S14
TO LOCK PULSE WAVEFORM SHAPING CIRCUIT 124

FIG.4

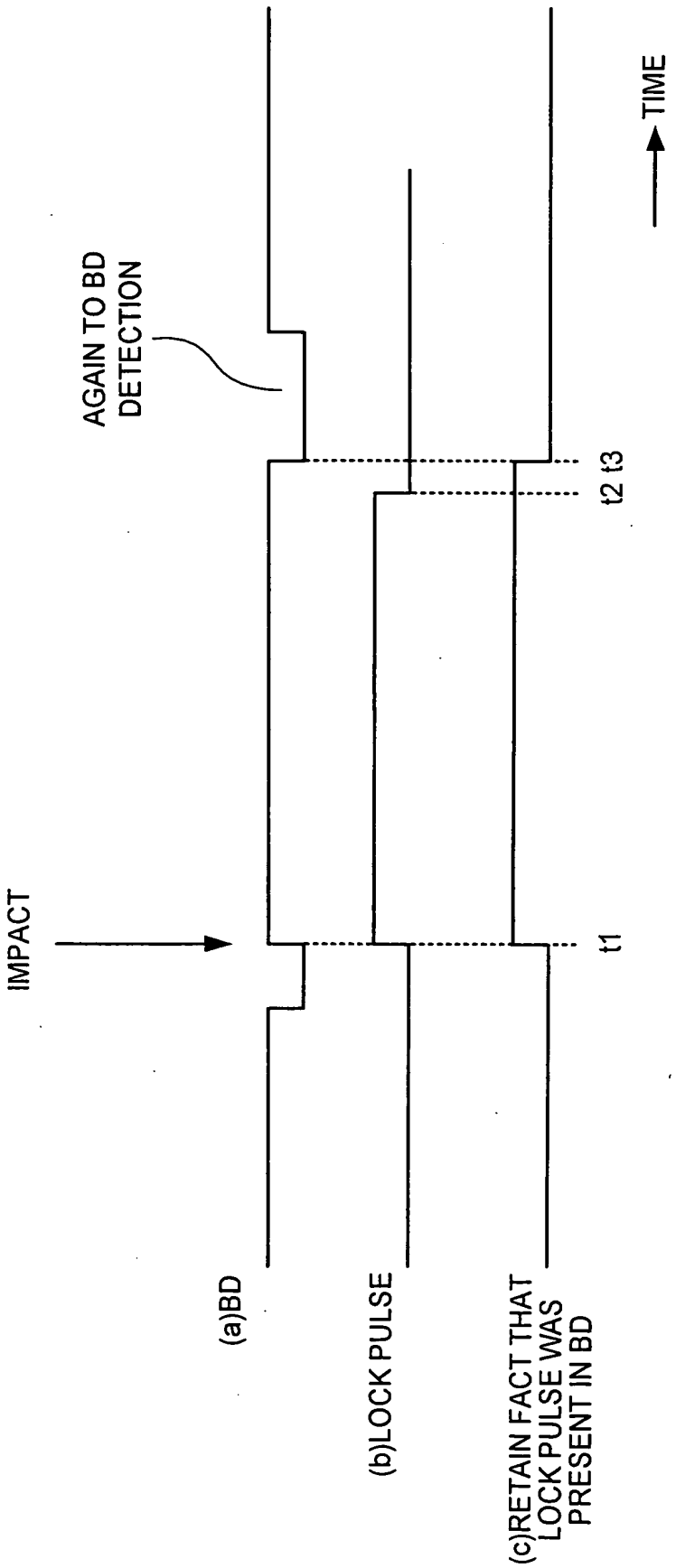
TIME
AGAIN TO BD DETECTION
IMPACT
t1
t2 t3
(a)BD
(b)LOCK PULSE
(c)RETAIN FACT THAT LOCK PULSE WAS PRESENT IN BD

FIG.5

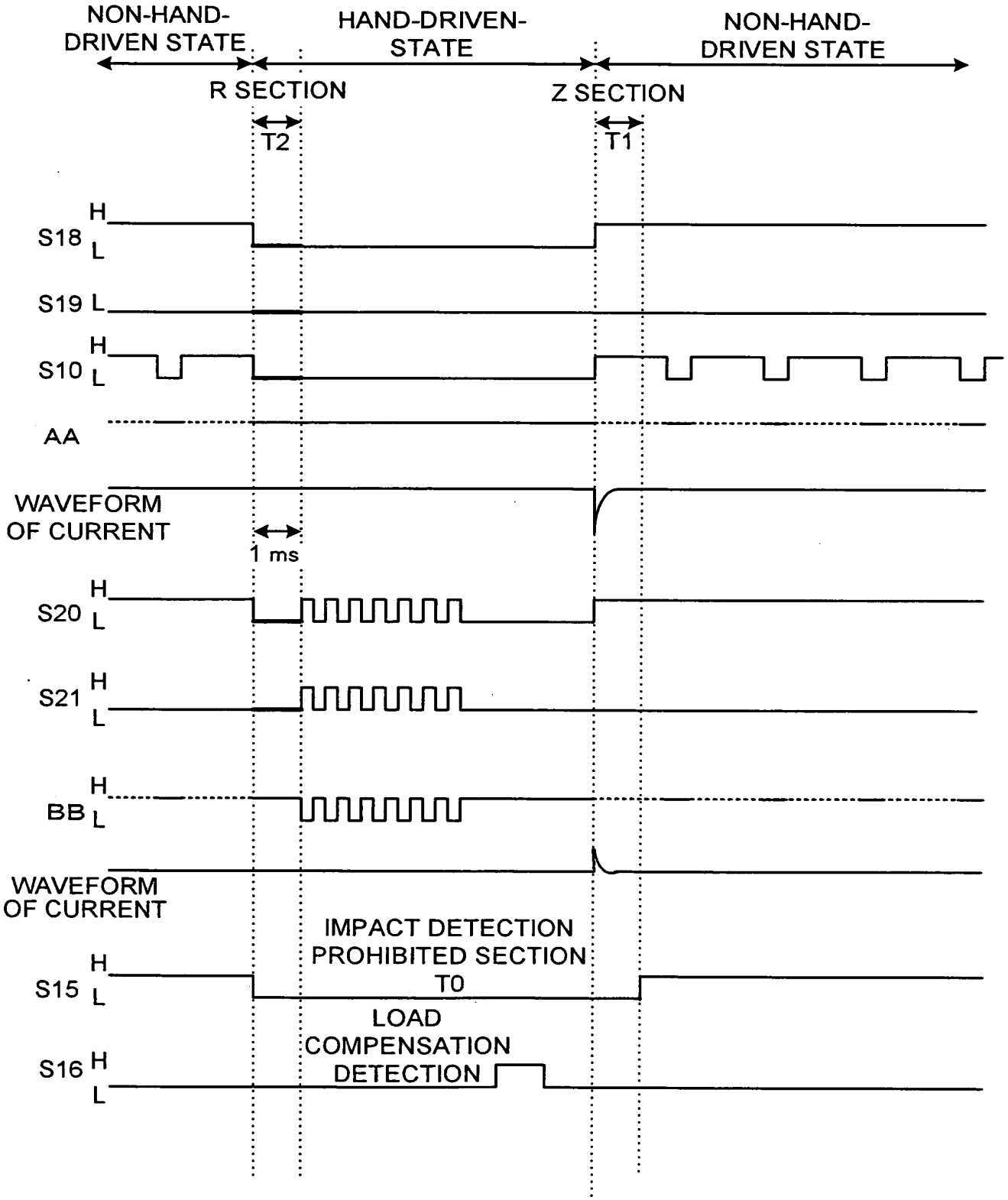
NON-HAND-DRIVEN STATE
HAND-DRIVEN-STATE
NON-HAND-DRIVEN STATE
R SECTION
Z SECTION
T2
T1
S18
S19
S10
AA
WAVEFORM OF CURRENT
1 ms
S20
S21
BB
WAVEFORM OF CURRENT
IMPACT DETECTION PROHIBITED SECTION
T0
S15
LOAD COMPENSATION DETECTION
S16
H
L

FIG.6

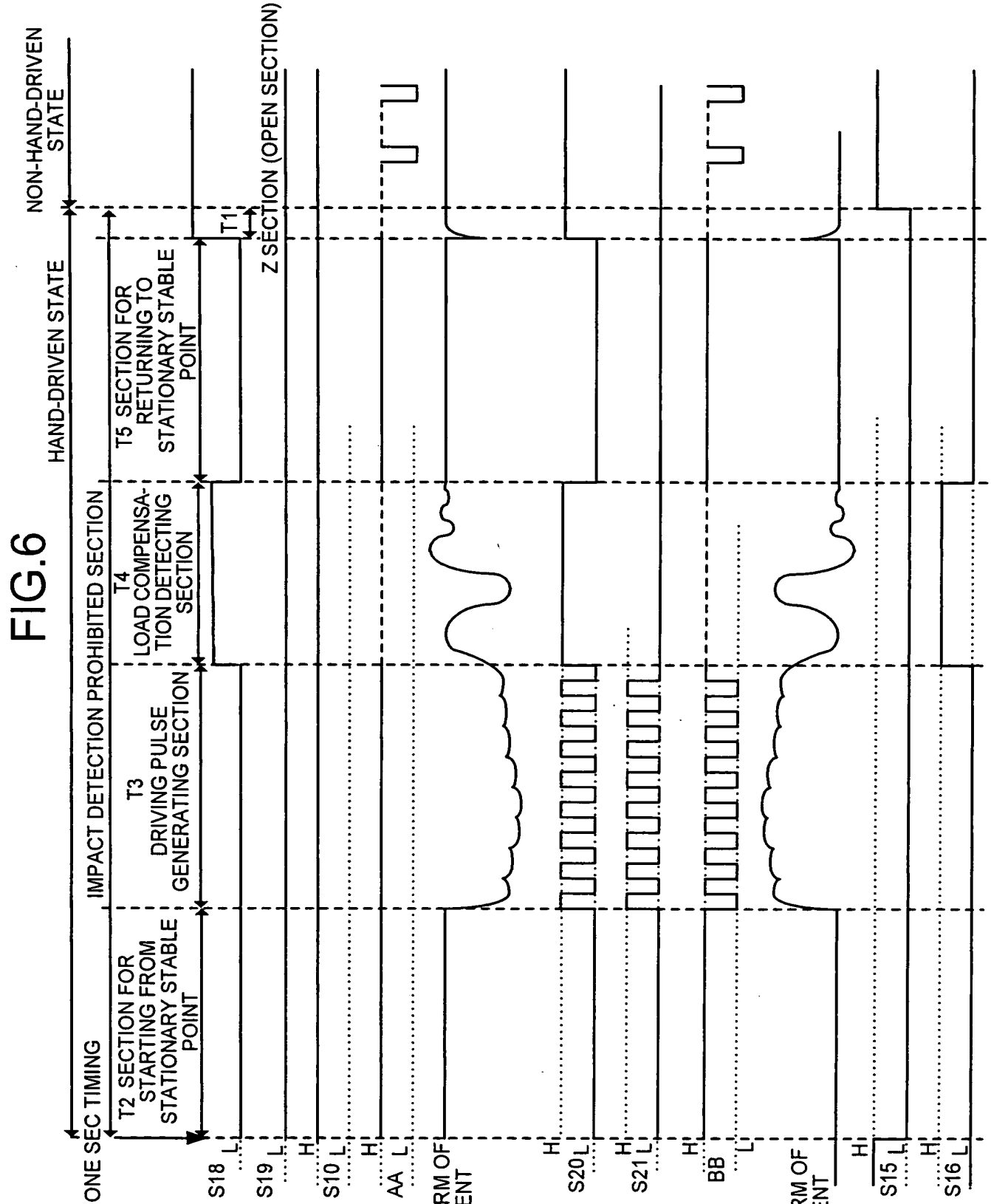
NON-HAND-DRIVEN STATE
HAND-DRIVEN STATE
IMPACT DETECTION PROHIBITED SECTION
ONE SEC TIMING
T2 SECTION FOR STARTING FROM STATIONARY STABLE POINT
T3 DRIVING PULSE GENERATING SECTION
T4 LOAD COMPENSATION DETECTING SECTION
T5 SECTION FOR RETURNING TO STATIONARY STABLE POINT
T1
Z SECTION (OPEN SECTION)
S18
S19
S10
AA
WAVEFORM OF CURRENT
S20
S21
BB
WAVEFORM OF CURRENT
S15
S16
H
L

FIG.7

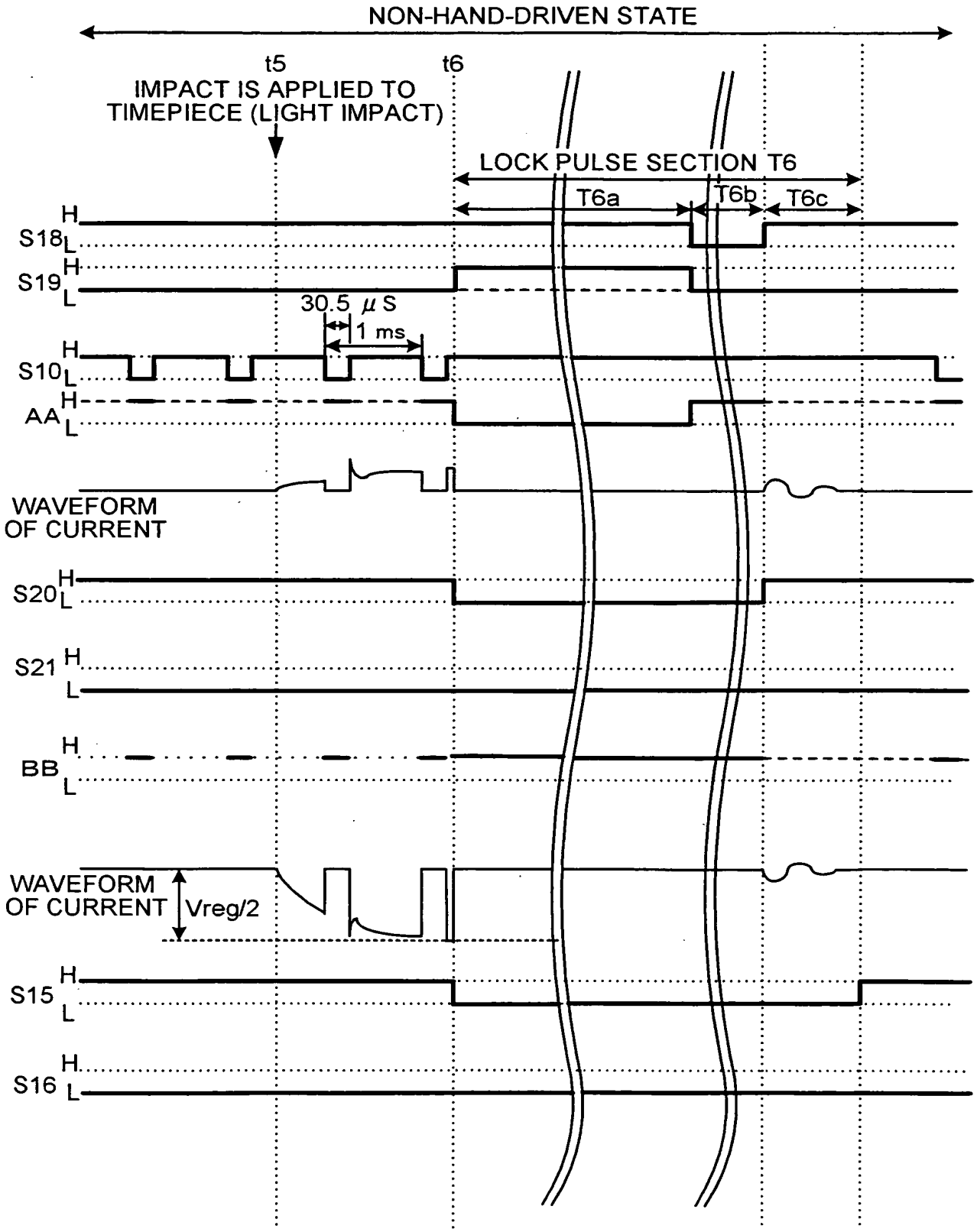
NON-HAND-DRIVEN STATE
t5
t6
IMPACT IS APPLIED TO TIMEPIECE (LIGHT IMPACT)
LOCK PULSE SECTION T6
T6a
T6b
T6c
S18
S19
30.5 μS
1 ms
S10
AA
WAVEFORM OF CURRENT
S20
S21
BB
WAVEFORM OF CURRENT
Vreg/2
S15
S16
H
L

FIG.8

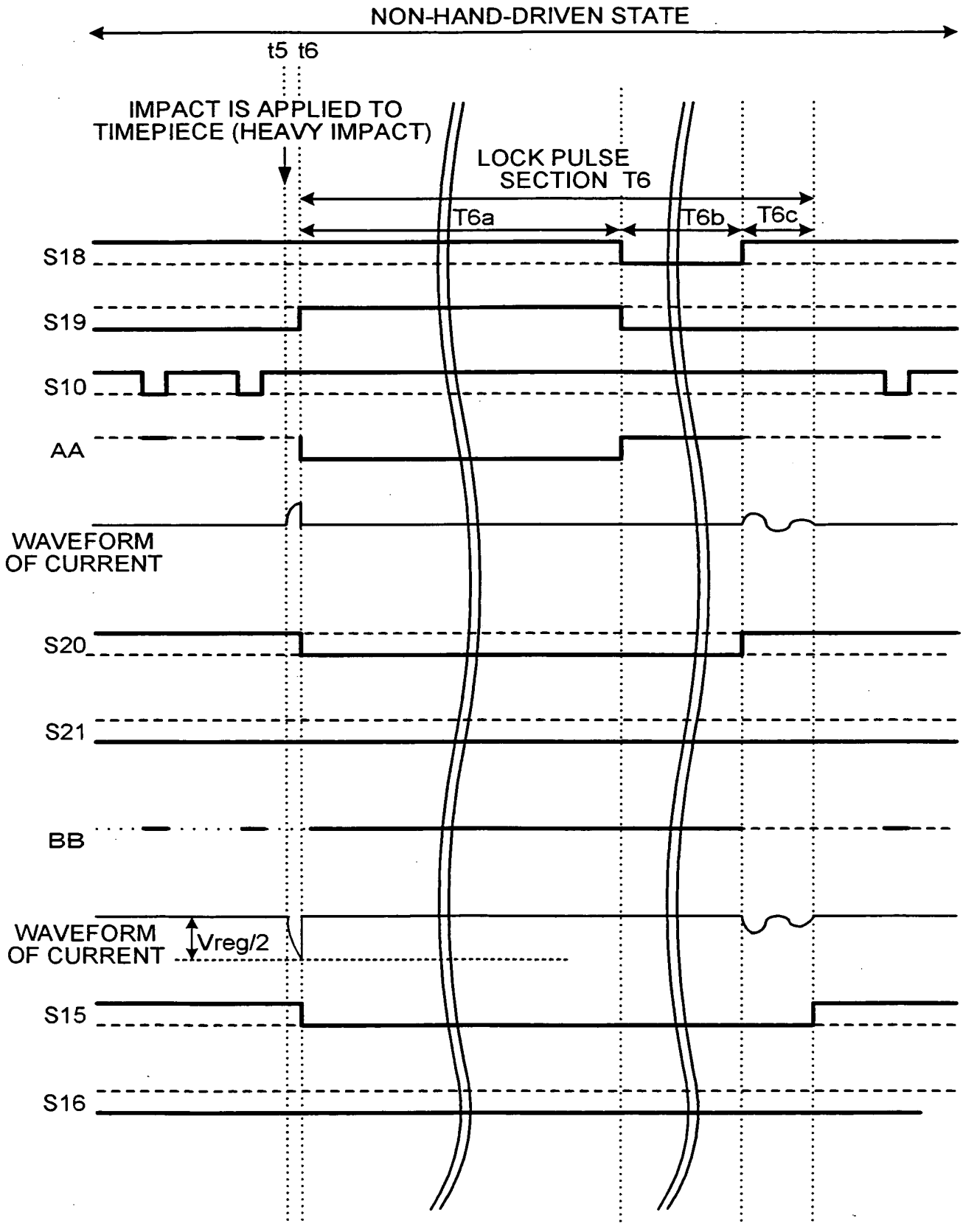
NON-HAND-DRIVEN STATE
t5
t6
IMPACT IS APPLIED TO TIMEPIECE (HEAVY IMPACT)
LOCK PULSE SECTION T6
T6a
T6b
T6c
S18
S19
S10
AA
WAVEFORM OF CURRENT
S20
S21
BB
WAVEFORM OF CURRENT
Vreg/2
S15
S16

FIG.9

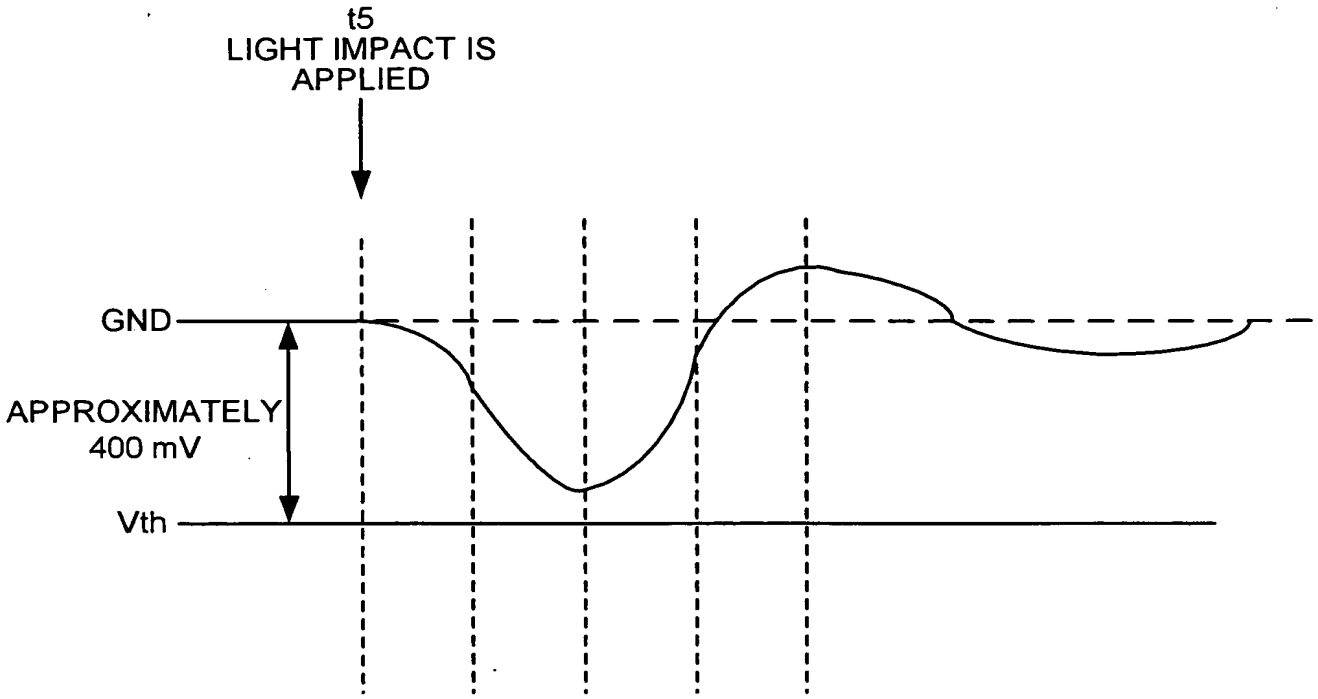
t5
LIGHT IMPACT IS
APPLIED
GND
APPROXIMATELY
400 mV
Vth

FIG.10

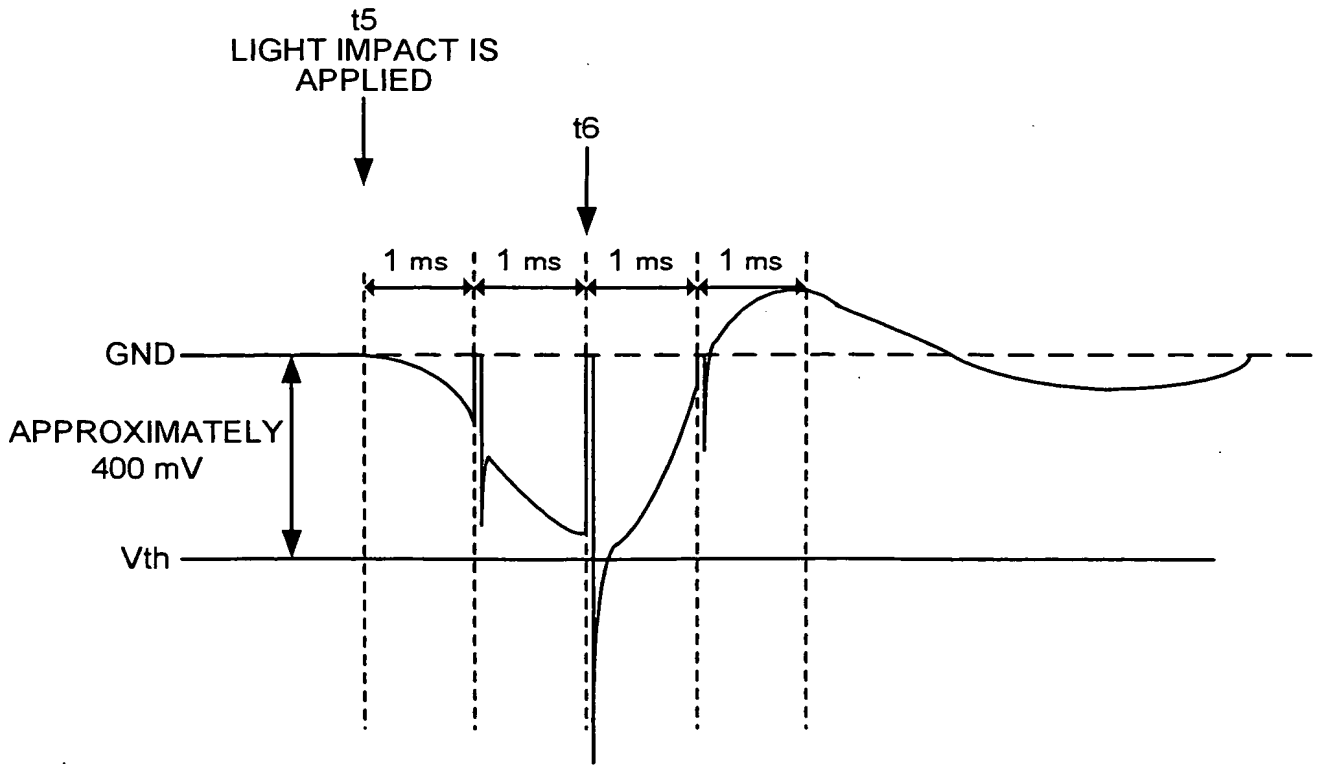
t5
LIGHT IMPACT IS
APPLIED
t6
1 ms
1 ms
1 ms
1 ms
GND
APPROXIMATELY
400 mV
Vth

FIG.11

PERIOD	CHOPPER-WIDTH	DETERMI-NATION	REMARK
2 ms	61 μS	×	WAVE-SHAPED BOOM GENERATED WHEN LIGHT IMPACT IS APPLIED LASTS APPROXIMATELY 2 MS AND DETECTION IS TOO LATE.
2 ms	30.5 μS	×	WAVE-SHAPED BOOM GENERATED WHEN LIGHT IMPACT IS APPLIED LASTS APPROXIMATELY 2 MS AND DETECTION IS TOO LATE.
1 ms	61 μS	×	TIME FROM RECEPTION TO DETECTION OF IMPACT (LIGHT IMPACT) IS AS SHORT AS 36 μS AND DETECTION IS IMPOSSIBLE WHEN IMPACT IS RECEIVED WITHIN CHOPPER.
1 ms	30.5 μS	O	BOTH OF DETECTION SENSITIVITY AND POWER CONSUMPTION ARE EXCELLENT
0.5 ms	61 μS	×	DETECTION SENSITIVITY IS MOST EXCELLENT, HOWEVER, POWER CONSUMPTION IS INCREASED BECAUSE CHOPPERS MOVE FAST.
0.5 ms	30.5 μS	×	DETECTION SENSITIVITY IS EXCELLENT, HOWEVER, POWER CONSUMPTION IS INCREASED BECAUSE CHOPPERS MOVE FAST.

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FIG.12

	30 cm	40 cm	50 cm	60 cm
1.8 (V)	OK	OK	OK	OK
1.7 (V)	OK	OK	OK	OK
1.6 (V)	OK	OK	OK	OK
1.5 (V)	TWO-SECOND DELAY	TWO-SECOND DELAY	TWO-SECOND DELAY	TWO-SECOND DELAY
1.4 (V)	TWO-SECOND DELAY	TWO-SECOND DELAY	TWO-SECOND DELAY	TWO-SECOND DELAY
1.35 (V)	OK	TWO-SECOND DELAY	TWO-SECOND DELAY	TWO-SECOND DELAY
1.25 (V)	TWO-SECOND DELAY	TWO-SECOND DELAY	—	—

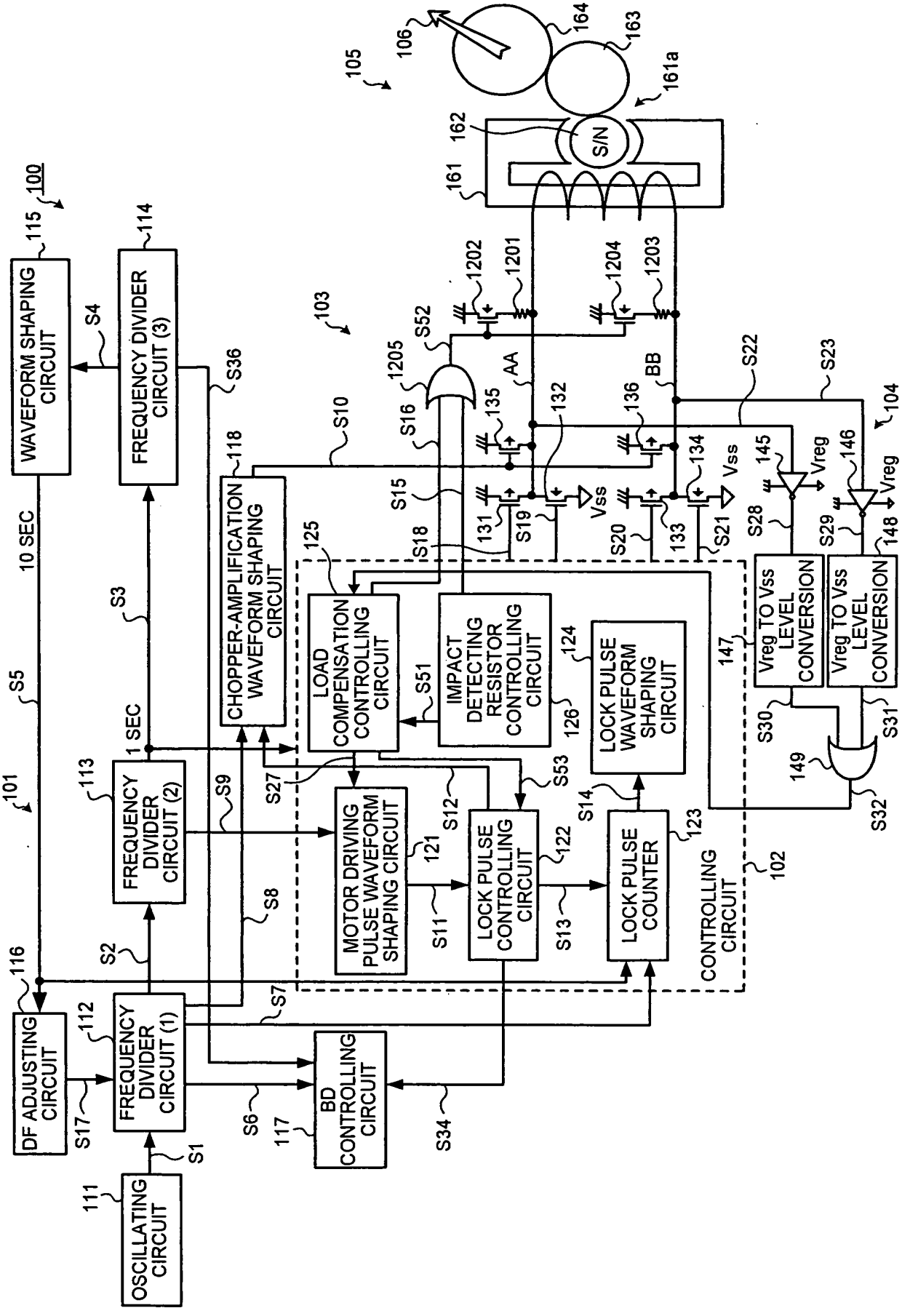
IMPACT DETECTING RESISTOR: 5 kΩ, LOCK PULSE SHAPE: LOCK TERM 5 ms, STABLE TERM 5 ms, INSENSITIVE TERM 1 ms
MOTOR DRIVERS: TWO HAND BIASED WEIGHT: 5 mgm

FIG.13

	30 cm	40 cm	50 cm	60 cm
1.8 (V)	OK	OK	OK	OK
1.7 (V)	OK	OK	OK	OK
1.6 (V)	OK	OK	OK	OK
1.5 (V)	OK	OK	OK	OK
1.4 (V)	OK	OK	OK	OK
1.35 (V)	OK	OK	OK	OK
1.25 (V)	OK	OK	OK	OK

IMPACT DETECTING RESISTOR: 5 kΩ, LOCK PULSE SHAPE: LOCK TERM 10 ms, STABLE TERM 5 ms, INSENSITIVE TERM 1 ms
MOTOR DRIVERS: TWO HAND BIASED WEIGHT: 5 mgm

FIG.14


100
101
102
103
104
105
106
111
112
113
114
115
116
117
118
121
122
123
124
125
126
131
132
133
134
135
136
147
148
149
161
161a
162
163
164
1201
1202
1203
1204
1205
AA
BB
S/N
Vss
Vreg
1 SEC
10 SEC
WAVEFORM SHAPING CIRCUIT
FREQUENCY DIVIDER CIRCUIT (3)
FREQUENCY DIVIDER CIRCUIT (2)
FREQUENCY DIVIDER CIRCUIT (1)
DF ADJUSTING CIRCUIT
OSCILLATING CIRCUIT
BD CONTROLLING CIRCUIT
CHOPPER-AMPLIFICATION WAVEFORM SHAPING CIRCUIT
LOAD COMPENSATION CONTROLLING CIRCUIT
IMPACT DETECTING RESISTOR CONTROLLING CIRCUIT
MOTOR DRIVING PULSE WAVEFORM SHAPING CIRCUIT
LOCK PULSE CONTROLLING CIRCUIT
LOCK PULSE COUNTER
LOCK PULSE WAVEFORM SHAPING CIRCUIT
Vreg TO Vss LEVEL CONVERSION
Vreg TO Vss LEVEL CONVERSION
CONTROLLING CIRCUIT
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
S14
S15
S16
S17
S18
S19
S20
S21
S22
S23
S27
S28
S29
S30
S31
S32
S34
S36
S51
S52
S53